REMARKS

Claims 18-25 are pending in this application. By this Amendment, the specification is amended. A substitute specification is attached. Claims 18-25 are added. Support for claims 18-25 is found at least at Figs. 1, 3a, 3b, 4, and 5 and pages 5-6 of the originally filed specification. Claims 1-17 are canceled without prejudice to, or disclaimer of, the subject matter recited in those claims. Reconsideration of the application based on the above amendments and the following remarks is respectfully requested.

The Office Action objects to the drawings for allegedly not showing every feature of the invention specified in the claims. The cancellation of claims 1-17 renders the objection moot.

The Office Action rejects claims 1-17 under 35 U.S.C. §112, second paragraph for allegedly being indefinite. The cancellation of claims 1-17 renders the objection moot. Claims 18-25 do not recite the alleged indefinite phrases, "n-channel region and p-channel region," or "an area of the substrate which separates the n-type source and n-type drain of the n-channel region." Accordingly, withdrawal of the rejection of claims 1-17 under 35 U.S.C. §112, second paragraph, is respectfully requested.

The Office Action objects to the specification for not having headings and for the title allegedly not being descriptive. A substitute specification is attached providing headings. The title has been changed. Accordingly, withdrawal of the objections is respectfully requested.

The Office Action rejects claims 1, 4-6, 8, 12, 14 and 15 under 35 U.S.C. §102(b) as being anticipated by GB 2-363,905 to Reedy et al. (hereinafter "Reedy"); and rejects claims 2, 3, 7, 9-11, 13, 16 and 17 as being unpatentable over Reedy in view of JP 53-149,770 to Takagi. The cancellation of claims 1-17 renders the rejection moot. The rejection is respectfully traversed to the extent it could be applied to new claims 18-25.

Claim 18 recites, among other features, a substrate having a channel region, a first p-type doped region, a second p-type doped region, a first n-type doped region and a second n-type doped region.

Reedy fails to teach or render obvious the above-recited features. Figs. 1 and 2 of Reedy show the channel and doped regions of a transistor formed as an island of layers above the surface of a substrate. Further, claim 1 of Reedy recites an island of semiconductor material on an insulating substrate. However, Reedy does not teach a substrate having a channel region, a first p-type doped region, a second p-type doped region, a first n-type doped region and a second n-type doped region, as recited in Applicant's claim 18.

Takagi fails to teach or render obvious the above recited feature. Similar to the device of Reedy, Figs. 1(a), 1(b) and 1(c) of Takagi show the channel and doped regions of a transistor as an island of layers formed above the surface of a substrate. However, Takagi does not teach a substrate having a channel region, a first p-type doped region, a second p-type doped region, a first n-type doped region and a second n-type doped region, as recited in claim 18.

The above-quoted feature has a structure that can be made part of a large-scale integration (LSI) arrangement. In addition, transistors having this structure can be made smaller relative to those made with thin-films.

In view of the above, Reedy cannot reasonably be considered to teach, or to render obvious, the combinations of all of the features positively recited in independent claim 18. Further, because Takagi is not applied in any manner that would overcome the above-identified shortfall in the application of Reedy to the subject matter of independent claim 18, to any extent that Reedy and Takagi are even combinable, a conclusion which applicants do not concede, no permissible combination of these references can reasonably be considered to render obvious the combinations of all of the features positively recited in claims 19-25, for at

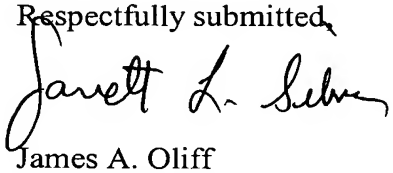
least the respective dependence of these claims directly on an allowable base claim, as well as the separate allowable subject matter that these claims recite.

Accordingly, withdrawal of the rejections of canceled claims 1-17, or claims 18-25 if applicable, under 35 U.S.C. §§102(b) and 103(a) as being anticipated by, or unpatentable over, the applied references are respectfully requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable consideration and prompt allowance of claims 18-25 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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Attachment:
Substitute Specification (Clean and Marked-Up Copies)

Date: September 29, 2008

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~~Semiconductor Device~~FIELD-EFFECT TRANSISTOR

FIELD OF THE INVENTION

The present invention relates to semiconductor devices, and in particular to semiconductor devices of a novel architecture which can be implemented as devices with a reduced device size. The present invention also relates to methods of operating such devices.

BACKGROUND OF THE INVENTION

One form of semiconductor device which, advantageously, can be implemented using the present invention is an inverter. An inverter is a circuit element which is in widespread use, particularly in logic applications. Such a circuit normally consists of two individual and complementary transistors, one n-channel and one p-channel transistor (such as MOS-FETs). Inverters may be configured with a variety of combinations for the arrangement of the transistor terminals. A common configuration is to have the gate terminals of the two individual transistors joined together, with the source terminal of one transistor connected to the drain terminal of the other transistor. A typical logic circuit application may typically include in excess of one thousand inverter circuits so the space occupied on the chip by these circuits can be significant.

The increase of device density in Large Scale Integration (LSI) or Ultra Large Scale Integration(ULSI) gives rise to an increasing need for a reduction of device size. Significant resources have been expended, both in research for new device structures and device production techniques, to achieve this goal, but reduction in device size remains as an ongoing requirement.